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Silicon solar cells with Low Environmental footprint and Advanced interfaces

SiLEAN - Deliverable report

D3.1. – nc-SiC:H TPC structure applied to full-sized wafers

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Project Scientific Abstract

The SiLEAN project deals with the development of advanced innovations to tackle the major drawbacks of silicon heterojunction solar cell technology, namely the high energy and material demand for Si wafer manufacturing, limited current generation, and the consumption of scarce materials like silver, bismuth and indium. Within the scope of the project, we will directly grow the wafers from the gas phase with low temperature processes, apply alternative passivation concepts that show higher optical transparency, develop indium-free contact layers and apply silver and bismuth-free metallization with all-in-one cell interconnection and encapsulation. The project aims to achieve >25.5% solar cell efficiency and >23.5% module efficiency with 50% lower costs for Si wafers and contacting, as well as up to 75% lower carbon footprint. All processes applied allow upscaling to larger sizes as well as high manufacturing throughput. Eventually, the developments of SiLEAN will pave the way for a new, lean, generation of heterojunction solar cell technology that will both increment the energy conversion efficiency and unlock production at terawatt-scale.

Public summary

Within the framework of the SiLEAN project, alternatives to highly absorptive silicon layers for the passivating and carrier-selective contact in silicon heterojunction (SHJ) solar cells are developed. One of the objectives of the project is to replace amorphous (a-Si:H) or nanocrystalline (nc-Si:H) silicon layers by thin-film materials that show excellent passivation and higher transparency at industrial wafer size. One such alternative is transparent passivating contact (TPC) architecture based on an ultra-thin (< 1.5 nm) silicon tunnel oxide (SiO_x) layer prepared by a wet-chemical process and n-type doped hydrogenated nanocrystalline silicon carbide (nc-SiC:H(n)) layer stacks fabricated by hot-wire chemical vapor deposition (HWCVD).

As a result of the deliverable, a stepwise optimization of the configuration of HWCVD process parameters, sample backing plate's (BP) material and amount as well as its preheating allowed to achieve a quite homogeneous and efficient passivation (minority-carrier lifetime ≈ 2.1 ms, implied open-circuit voltage (iV_{oc}) ≈ 740 mV at the center of a sample) of industrially relevant M2+ size Cz c-Si wafers by Transparent Passivating Contact (TPC) consisting of double-layer nc-SiC:H(n)/SiO_x stack. In this case, lab-scale 2x2 cm^2 TPC based solar cells showed an increased short-circuit current density of up to 40.0 mA/cm^2. This value is about 0.6 mA/cm^2 higher than that of conventional SHJ reference cells.

Further attempts on optimization of passivation properties and their homogeneity will be made by using highly doped Cz c-Si wafers as BPs. The optimum trade-off between open-circuit voltage (V_{oc}) and fill factor (FF) will be found with ranging nc-SiC:H(n) passivating layer thickness. Next, TPC on full M2+ size solar cells using high-quality epitaxially grown wafers will be tested.

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Project partners:

#	Partner short name	Partner Full Name
1	FZJ	FORSCHUNGSZENTRUM JULICH GMBH
2	IMEC	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM
3	TUD	TECHNISCHE UNIVERSITEIT DELFT
4	UNR	UNIRESEARCH BV
5	NXW	NEXWAFE GMBH
6	PVW	PV Works B.V.
7	GET	GraphEnergyTech
8	3SUN	3SUN S.R.L.
9	GUNAM	ODTU GUNES ENERJISI UYGULAMA VE ARASTIRMA MERKEZI

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