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Silicon solar cells with Low Environmental footprint and Advanced interfaces

SiLEAN - Deliverable report

D3.2 – TMO structure applied to full-sized wafers

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Project Scientific Abstract

The SiLEAN project deals with the development of advanced innovations to tackle the major drawbacks of silicon heterojunction solar cell technology, namely the high energy and material demand for Si wafer manufacturing, limited current generation, and the consumption of scarce materials like silver, bismuth and indium. Within the scope of the project, we will directly grow the wafers from the gas phase with low temperature processes, apply alternative passivation concepts that show higher optical transparency, develop indium-free contact layers and apply silver and bismuth-free metallization with all-in-one cell interconnection and encapsulation. The project aims to achieve >25.5% solar cell efficiency and >23.5% module efficiency with 50% lower costs for Si wafers and contacting, as well as up to 75% lower carbon footprint. All processes applied allow upscaling to larger sizes as well as high manufacturing throughput. Eventually, the developments of SiLEAN will pave the way for a new, lean, generation of heterojunction solar cell technology that will both increment the energy conversion efficiency and unlock production at terawatt-scale.

Public summary

Silicon heterojunction (SHJ) is one of the most promising photovoltaic technologies, and it has achieved a world record efficiency of 27.81% [1]. However, doped Si-based thin-film layers placed at the illuminated side of SHJ solar cells induce parasitic absorption losses and thereby limit the achievable short-circuit current density. To mitigate these losses, transition metal oxide (TMO) materials, particularly molybdenum oxide (MoO_x)—which exhibits a high work function that enables effective hole selectivity and excellent transparency—has been utilized in SHJ solar cells as a replacement of p-type Si-based thin-film layers [2]. In this study, MoO_x layers were deposited using both thermal evaporation and sputtering techniques on lab-scale c-Si wafers.

Applying the thermal evaporation method, 23.94% power conversion efficiency has been achieved on 4-inch wafer for MoO_X-based SHJ solar cell with 4-inch-compatible tools. When employing M2-compatible tools—that are closer to industrial standards—an efficiency of 22.03% was obtained on a 4-inch wafer without plasma treatment (PT). However, further optimization of deposition parameters for each layer is still required. Initial results for 2×2 cm^2 cells on M2+ wafer reached an efficiency of 14.48% in the first run using screen printing. Note that M2+ and 4-inch wafers differ in terms of thickness, resistivity, and metallization methods, and the process needs to be further optimized.

Using the sputtering method, currently a maximum efficiency of 21.60% has been achieved for 4-inch MoO_X-based SHJ solar cells with plasma treatment with Boron (PTB). To minimize the sputtering damage, sputtering parameters including argon flow, sputtering power, and power supply (DC or RF), interface treatments and the underlying hydrogenated intrinsic amorphous silicon ((i)a-Si:H) film were optimized. The precursors prepared with optimized deposition parameters demonstrated promising carrier lifetime and implied V_{OC} (iV_{OC}), significantly mitigating sputtering-induced damage.

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Project partners:

#	Partner short name	Partner Full Name
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2	IMEC	INTERUNIVERSITAIR MICRO-ELECTRONICA CENTRUM
3	TUD	TECHNISCHE UNIVERSITEIT DELFT
4	UNR	UNIRESEARCH BV
5	NXW	NEXWAFE GMBH
6	PVW	PV Works B.V.
7	GET	GraphEnergyTech
8	3SUN	3SUN S.R.L.
9	GUNAM	ODTÜ-GÜNAM

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